

Breakdown of Gate Oxides During Irradiation with Heavy Ions[†]

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Abstract

Breakdown of thin gate oxides from heavy ions is investigated using capacitor test structures. Soft breakdown was observed for 45 Å oxides, but not for 75 Å oxides. Lower critical fields were observed when experiments were done with high fluences during each successive step. This implies that oxide defects play an important role in breakdown from heavy ions and that breakdown occurs more readily when an ion strike occurs close to a defect site. Critical fields for 75 Å oxides are low enough to allow gate rupture to occur at normal supply voltages for ions with high LET.

I. INTRODUCTION

Although gate rupture of power MOSFETs from heavy ions has been studied for many years, such effects have only recently been observed in high-density digital circuits which have much thinner oxides. Permanent damage attributed to catastrophic gate breakdown from heavy ions was first reported in 1994 for 4-Mb DRAMs [1]. Later work showed that similar effects occur in the oxide-nitride sandwich structure used in programmable gate arrays [2]. It is important to note that breakdown from heavy ions occurred in both types of structures when they were biased at normal operating voltages. Although the threshold LET for breakdown to occur was well beyond the "iron threshold" in the galactic cosmic ray spectrum, data on DRAMs showed that the threshold for damage was lower for scaled devices, with higher electric fields across the insulator structure. The issue of how scaling affects catastrophic damage to the gate regions of VLSI devices, and how the mechanisms for damage relate to processing controls and oxide defects, is a complex issue which is still being investigated.

Last year, Sexton, et al. reported the results of a study of breakdown in capacitor structures, along with a more limited evaluation of breakdown effects in static memories [3]. Most of the devices that they studied had thinner gate oxides than the devices in the initial studies in References 1 and 2, and Sexton, et al. concluded that the gate rupture problem would be less severe for highly scaled devices with thin gates.

The present paper extends the earlier work on breakdown effects, including new factors such as the dominance of soft breakdown rather than hard breakdown in oxides below 60 Å, and the dependence of the critical field on fluence. Experimental results on capacitors from a different fabrication process were observed to have lower critical breakdown fields than reported in Reference 3.

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Breakdown in the present capacitor structures occurred with applied voltages that were within the range of electric fields expected for scaled devices. Possible reasons for the differences in experimental results are discussed, along with evidence for the likely role of oxide defects in the gate-rupture process.

II. BASIC CONSIDERATIONS

A. Capacitors vs. Integrated Circuit Structures

There are important differences between capacitor test structures and integrated circuits that must be taken into account when evaluating gate rupture effects. Although capacitors provide certain advantages, several complications arise when one attempts to extend capacitor results to circuits. The main advantage of capacitor test structures is that they provide explicit control of the electric field across the oxide, over a wide range. For most circuits, the field can only be changed over a limited range, imposed by circuit power supply voltage limitations. However, VLSI circuits can be viewed as a very large number of "test structures" within a single package, with the inherent ability to measure many different breakdown events, and statistical distributions of gate-rupture failures on a single device [1,2]. In most cases, only a single breakdown event can be observed on individual capacitors. This severely limits the ability to determine the statistical variability of gate rupture effects on capacitors unless very large numbers of capacitors are available.

The area of capacitor structures also plays an important role. In most cases the area of individual capacitors is many times larger than that of individual MOS transistors, but significantly lower than the total gate area of all MOS devices on a large-scale device. Other differences between capacitors and VLSI devices that are potentially important for gate rupture are shown in Table 1.

Table 1
Features of Capacitors and VLSI Devices of Importance
in Oxide Rupture Studies

	Oxide Field	Number of Events	Perimeter to Area Ratio	Lateral Field
VLSI Devices	Limited by circuit operating voltage range	Many on a single device	Very large	Present
Capacitors	Can be directly controlled	Usually one	Small	None

The doping level of the silicon underneath the oxide may also be important because it affects the magnitude and time response of transient currents (and the voltages within the underlying silicon region that result from those currents) [4,5]. The capacitors that were tested in Reference 3 and those tested in the present work were all fabricated over very lightly doped silicon regions ($\sim 10^{15} \text{ cm}^{-3}$). Doping levels beneath the gate region of MOS devices are one-to-two orders of magnitude higher [6,7], and it is possible that capacitor results on more lightly doped material may be different from the gate rupture tolerance of the same oxides over material with higher doping levels.

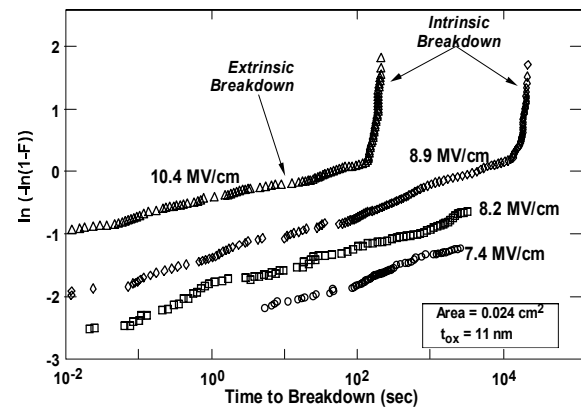
Another potentially important difference between capacitors and actual gate regions is the perimeter area ratio which is three-to-four orders of magnitude higher for individual gates than for capacitors. Edge effects – which may be influenced by the nonplanar nature of silicon and oxides near the periphery – are clearly different for capacitors and MOS transistors.

B. Time-Dependent Dielectric Breakdown

Oxide quality is often measured by comparing intrinsic breakdown, measured over short time periods by applying a voltage ramp. Recent studies of time-dependent dielectric breakdown (TDDB) have shown that the breakdown characteristics of thin oxides with intermediate-to-large area are dominated by the distribution of impurities within the oxide [8], not the intrinsic breakdown strength. This results in a much lower effective dielectric strength than indicated by intrinsic breakdown. Figure 1 shows some results from that study, done on capacitors with an oxide thickness of 110 Å. The results can be fitted to a bimodal Weibull distribution (the parameter F is the cumulative number of errors). Intrinsic and extrinsic regions are shown. For short time periods, or for capacitors with small area, intrinsic breakdown -- the steep region where all of the capacitors will break down if they are biased for a specific time interval -- is dominant. (Note that although there are a small number of capacitors that break in the extrinsic region at 10.4 MV/cm, the majority break in the intrinsic region). For longer time periods, or for capacitors with large area, extrinsic breakdown -- related to defects in the oxide -- is the dominant contribution. In that case breakdown occurs at much lower field strength, but only as a result of extrinsic defects.

The area of the capacitors used in Figure 1 is slightly more than twice that of the largest capacitors in our test structures. However, the oxide thickness is somewhat thicker. A more recent paper has shown that extrinsic breakdown is even more important for TDDB in thin oxides [9]. This work reported a much stronger dependence of charge-to-breakdown on area for thin oxides compared to thicker oxides. The difference was much stronger for 43 Å oxides than for oxides between 63 and 110 Å. This work indicates that extrinsic breakdown will continue to be important for very thin oxides.[†]

[†]Extrinsic breakdown is only important for thin oxides, less than approximately 200 Å [10]. Intrinsic breakdown is expected to dominate for thicker oxides such as those used in power MOSFETs. Figure 1. Field dependence of intrinsic and extrinsic time-dependent dielectric breakdown (after Ref. 8)



TDDB involves constant stress at a fixed voltage, and the mechanisms for TDDB are not directly related to gate rupture from heavy ions (TDDB stresses the entire oxide, whereas the passage of a heavy ion only produces charge in a single, localized region).

However, the TDDB work is important because gate rupture tests are in fact an *admixture* of a moderate-duration TDDB test with the effects of randomly occurring, short-duration pulses from heavy ions. The TDDB work suggests (1) an inherent time dependence, i.e., that heavy-ion results may be different if the tests are done over longer time periods where the extrinsic breakdown features dominate; and (2) the possibility that heavy ion results may also depend on fluence if impurities are involved in the breakdown process, because ions that strike within some neighborhood of an oxide defect may produce breakdown at lower fields than oxides that strike regions of the oxide where no defects are present.

The gate rupture studies done to date on devices with thin oxides appear to require fluences such that there are several ion hits -- ~ 10 to 1000 -- on each oxide region before breakdown occurs.[†] This suggests that the extrinsic defect distribution may play a role in the gate rupture process. Mechanisms that cause defects to affect oxide breakdown are outside the scope of this paper, but are discussed in the literature [8-15].

III. EXPERIMENTAL RESULTS

A. Test Structures and Devices

Capacitors with two oxide thicknesses were used in this study, 45 and 75 Å. The capacitors were fabricated by MIT Lincoln Laboratories. The surface conductor (corresponding to the gate of a CMOS process) was doped polysilicon, with an n-substrate, doped to approximately 10^{15} cm^{-3} . The resistivity of the underlying substrate is about the same as

[†]It is only possible to determine the number of ions for failure on capacitors when they are continually monitored during irradiation. Circuit level tests provide this information indirectly because many breakdown events can be established on individual devices that of the capacitors used in Reference 3, considerably lower than the doping level of the channel in MOS transistors.

Capacitors were available for both oxide thicknesses with four different areas, from 1.2×10^{-3} to 1.1×10^{-2} cm². Each test chip contained several different capacitor geometries. Breakdown fields were typically 11.6 MV/cm, as measured by Lincoln Laboratory using a ramp voltage (1.6 V/sec).

Experiments were also done on power MOSFETs from International Rectifier. The oxide thickness of those devices was 750 Å. Power MOSFETs with several different voltage ratings – 100 to 400 volts -- were used; the doping levels of the underlying regions varied from 4×10^{14} to 3×10^{15} cm⁻³. Including the power MOSFETs in the study allowed breakdown in thick oxides to be compared to breakdown in the much thinner oxides that are representative of integrated circuits. It also allowed the effects of the underlying doping level on breakdown to be determined, at least for thick oxides, as well as providing a connection to gate rupture effects in power MOSFETs, which have been more thoroughly investigated [15]. Power MOSFETs were treated like the capacitors during the tests, applying voltage only to the gate during testing (the source and drain were grounded).

B. Experimental Procedure

Breakdown experiments were done by applying a constant bias to the capacitor, continually monitoring the capacitor voltage during the irradiation. Voltage on the capacitors was measured with a digital voltmeter, buffered by an operational amplifier. Voltage resolution was 1 mV, with a compliance limit of 10 mA. Currents as low as 200 nA could be measured. Tests were done at the Brookhaven National Laboratory Van de Graaff accelerator. Beam current was monitored to make sure that it remained stable during each run.

Initial experiments were done using a fluence such that about 2000 ions would strike the capacitor before each test sequence was concluded, adjusting the beam flux and run times so that approximately the same number of ions struck each capacitor during each test run (the beam flux was adjusted to maintain the same fluence for capacitors with different area). Each run was about two minutes. If no breakdown occurred during that time, then the voltage was increased, and the experiment was repeated. Voltage steps of 0.1 or 0.2 V were used. Step size was limited by the available experimental time at the accelerator, which restricted the total number of runs, not by instrumentation accuracy. All irradiations were done using ions at normal incidence. There was no evidence that noise or interaction from the experimental apparatus interfered with the breakdown measurements. The voltage at which breakdown occurred when the ion beam impinged on the devices was much lower than the voltage at which the devices would fail from static stressing.

Later tests were done using much higher fluences, increasing the number of ions that struck each capacitor to about 80,000 per test run in order to compare breakdown effects at high and low fluences. These runs were typically completed in 10 to 15 minutes, approximately five times longer than the runs at low fluences.

Capacitors were irradiated in groups of four devices (with the same area for each individual device). Measurements were

made continually during irradiation, providing approximately 0.1 second resolution of the time at which failure occurred. Power MOSFETs were irradiated individually using an HP4142 measurement system with higher voltage range than that provided by the buffers used in the capacitor experiments. Measurements of the power MOSFETs were made during the irradiation, just as for the thin capacitor structures.

C. Initial Results at Intermediate Fluences

Results of the tests with heavy ions are shown in Figure 2 for test structures with the two oxide thicknesses. The ordinate shows the critical field (MV/cm), which was corrected for built-in potential. Our results showed that the field strength required to initiate breakdown was higher for the thinner capacitors, in general agreement with the trend of results in Reference 3. However, comparing devices with similar oxide thickness, the electric field strength was somewhat lower for the capacitors in our study than for those in the earlier study. Table 2 compares the results at an LET of 60 MeV-cm²/mg for our work and the results from the Sandia group [3].

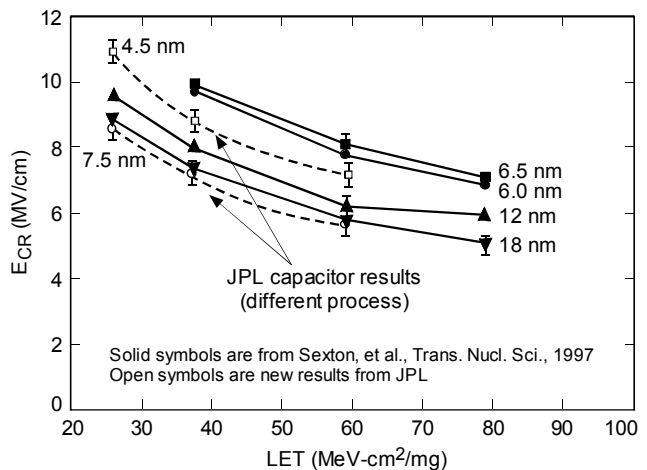


Figure 2. Dependence of critical field on linear energy transfer for oxides with different thickness.

Table 2
Comparison of Oxide Gate Rupture Results for Capacitors

Oxide Thickness (Å)	Critical Field @ LET = 60 (MV/cm)	Estimated Number of Ions Striking Capacitor per Run	Data Source
45	7.2	2000	Current work
60	7.8	not specified	Reference 3
65	8.2	130	Reference 3
75	5.7	2000	Current work
120	6.6	130	Reference 3
180	5.9	130	Reference 3

It is possible that the lower critical fields in our study could be entirely due to differences in processing. However, Sexton et al. also observed that the voltage for breakdown in a 256-kB (commercial) SRAM with a 133 Å oxide was

somewhat lower than the critical voltage for their 120 Å capacitors, comparable to the relative differences in field strength observed between our capacitors and those from Sandia. Much smaller differences between the capacitor and circuit results occurred for a 16-kB SRAM test structure (with less total oxide area than the 256k SRAM) in their work. This raises the possibility that differences in the test approach and capacitor areas may be a factor in the differences between the various tests. As shown in the table, the number of ions striking each capacitor during each test cycle was approximately an order of magnitude larger for our tests than in the work of Reference 3.

The 45 Å oxide in our study is much thinner than the oxides studied previously by Sexton, et al. Breakdown in the 45 Å oxides exhibited a different signature – soft breakdown – compared to the 75 Å capacitors. Figure 3 shows two examples, taken simultaneously during the same run; both devices were located on the same test chip. One device exhibited an abrupt change in voltage, but did not behave like a thick oxide in that the current was limited to about 120 µA instead of increasing to near short-circuit conditions (a signature of soft breakdown). Increasing the applied voltage after breakdown occurred caused only a small incremental change in current; thus, the breakdown was essentially current limited to about 120 µA by the properties of the damaged region, not the measurement circuitry. This is similar to soft breakdown characteristics reported in reliability studies for thin oxides [11,12], and is much different from the near short circuit behavior that is usually seen for thick oxides.

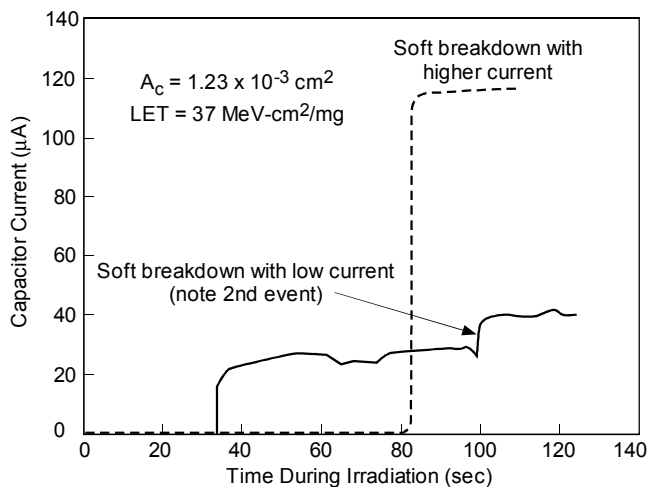


Figure 3. Soft breakdown characteristics observed for 45 Å capacitors (both capacitors were on the same chip, and irradiated simultaneously).

The 75 Å devices were tested with the same hardware, and generally exhibited current increases of about 1 mA (ultimately limited by the 10 mA compliance of the measurement circuit). The current increased further when the voltage across the capacitor was raised after breakdown occurred. Thus, the breakdown signature was quite different for the two different oxides, but consistent with reliability work on oxides with similar thicknesses. Neither of the oxides exhibited true oxide “shorts,” but breakdown in the thinner oxides produced much lower current conditions (at fixed bias) after breakdown occurred.

Even more unusual behavior occurred for some of the 45 Å devices. The second curve in Figure 3 shows a still lower current breakdown characteristic, limited to about 30 µA. Some noise-like instability was evident after breakdown. As the irradiation continued, a second breakdown event occurred in this same structure with an incremental step of only 10 µA.

Such multiple events were frequently observed for the 45 Å capacitors. This type of soft breakdown has also been reported in TDDDB studies of oxide breakdown, and generally occurs only for oxides with thicknesses below 50 Å [11-13]. It severely complicates the interpretation of gate rupture experiments in thin oxides. The currents are low, and the nature of the breakdown is completely different from that of thicker oxides which have a steep “knee” region and generally result in catastrophic breakdown. Although the currents that occur in soft breakdown are low from the standpoint of measuring them with conventional instrumentation, they are very large currents in the context of the drive current capability of small-area MOSFETs, and would cause failures in most circuits.

D. Fluence Dependence

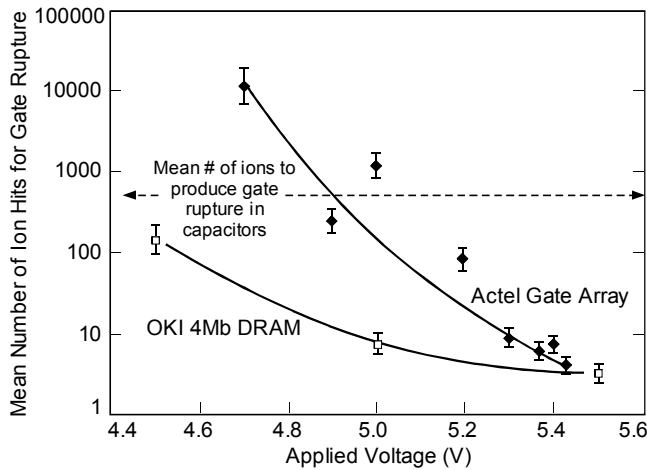
The number of ions required for gate rupture in earlier work [1,2] has been determined, and is shown in Figure 4 along with the new results in this study at intermediate fluences. An average of several hundred to several thousand average “hits” on the total insulator area was required to initiate insulator rupture at moderate field strengths. Even when the electric field was increased many hits were still required for breakdown to occur. It is apparent from these results that the field strength at which breakdown occurs during an experiment will depend on the number of ions that impinge on the insulator area during the run. Note that it is only possible to compare the mean number of ions for breakdown in capacitors because capacitor breakdown involves only one event per structure, unlike the integrated circuit results that provide many events per structure.

Unless experiments with capacitors at moderate fields use a sufficient number of ions, breakdown will not occur, and the critical field will be overestimated. The circuit results imply that differences of about 20% can occur between experiments with low numbers of ions and experiments with high numbers of ions, assuming comparable voltage dependence for the heavy-ion breakdown process.

The statistical nature of the accelerator ion beam must also be considered, particularly when the mean number of ions passing through the total physical area is small. The flux of ions during an experiment is simply an average, and the exact number will vary statistically. However, the results of several experiments (such as those for the Actel gate array in Figure 4) clearly show that the fields are not yet high enough to get a one-to-one correspondence between ion strikes and breakdown events.

Figure 4. Mean number of ions striking the active insulator area (from breakdown studies at the circuit level in references 1 and 2)

The fact that breakdown appears to require multiple “hits” can be interpreted several ways. It is possible that breakdown



may be the result of a gradual “weakening” of the oxide by a succession of ion strikes, or simply that some localized regions within the oxide are more sensitive to the breakdown process. In the latter case, breakdown will depend on the probability that an ion strikes near a defect site. This will be discussed further in the next section.

Additional experiments were done using much higher fluences in order to see how the critical voltage would be affected by fluence. Figure 5 shows how the voltage for breakdown compared for 75 Å capacitors at an LET of 37 MeV-cm²/mg. The mean voltage for failure decreased by about 7% at higher fluences. The only difference in these experiments was the fluence used for each test sequence.

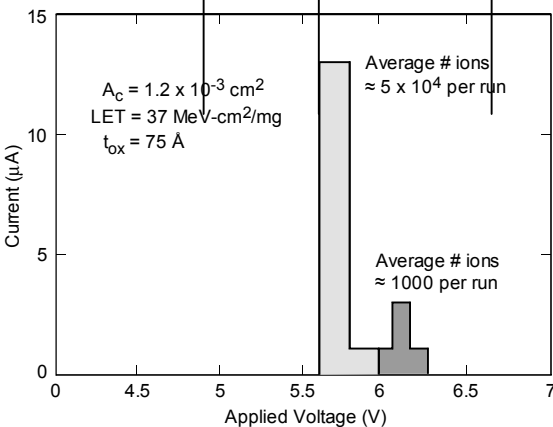
Figure 5. Mean breakdown voltage for 75 Å capacitors with two different fluence conditions during successive irradiation cycles.

E. Influence of Doping Levels

Spreading resistance measurements were used to determine the doping density of the epitaxial region of the power MOSFETs. Gate oxide thicknesses were measured with a scanning electron microscope (using “sectioned” devices that had been sawed and lapped). All three MOSFET types had identical gate thicknesses, 750 Å; the measurement uncertainty was less than 40 Å. Their doping levels and epitaxial thicknesses are shown in Table 3.

Table 3
Properties of the Power MOSFETs

Type	Rated Drain-Source Voltage	Doping Level	Epitaxial Thickness
2N6782	100 V	$3 \times 10^{15} \text{ cm}^{-3}$	15 μm



2N6790	200 V	$1 \times 10^{15} \text{ cm}^{-3}$	26 μm
2N6786	400 V	$4 \times 10^{14} \text{ cm}^{-3}$	40 μm

Measurements of the gate-source voltage required for breakdown were done by subjecting each device to a series of irradiations. A fluence of approximately 5×10^4 ions/cm² was used for each radiation run (an “intermediate fluence” condition). The voltage was increased in one-volt steps for each successive irradiation, continuing the irradiation sequence until failure occurred. There were significant differences in the voltage at which breakdown occurred for the different device types, as shown in Figure 6. Three devices of each type were irradiated with each ion. The breakdown voltage was very consistent for units of the same type (the error bars show the range of data for the three devices). These results imply that the critical voltage condition for breakdown is somewhat lower for higher doping concentrations than for low doping. Although the change in voltage may appear small, it raises the possibility that the critical field may be lower by 10% or more for devices with higher doping levels. That could have a significant impact on conclusions about critical fields and device operating voltage limits, particularly for highly scaled devices.

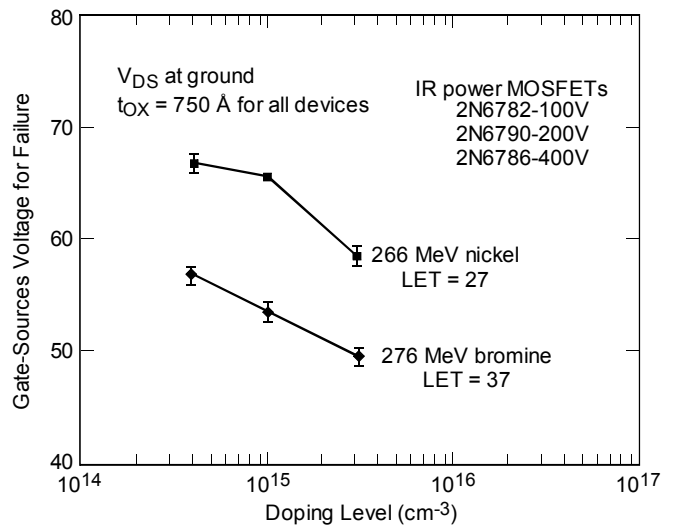


Figure 6. Critical voltage for gate-source breakdown for the three different power MOSFET types. All three have identical oxides (750 Å), but have different doping densities in the silicon region beneath the gate.

This result may not be directly applicable to highly scaled MOSFETs because the depth of the underlying silicon region is so much smaller. However, the thickness of the underlying region for the 100 V devices is only 15 μm , compared to 40 μm for the 400 V device. One would normally expect that the thinner region would have less impact on the critical voltage for gate rupture, not more impact, because the depletion width (and funneling depth) are lower. If the critical field for structures with light doping densities is higher, then breakdown may occur at lower fields in devices with higher doping densities, affecting conclusions about critical fields in scaled devices. This issue needs to be investigated more thoroughly for devices with shallow structures.

IV. DISCUSSION

A. Sensitive Dimensions

The fact that the first ion generally does not initiate breakdown implies that the breakdown process is related to the probability of an ion striking close to an oxide defect site. Although it is possible that multiple events in close proximity are required to produce breakdown, we have compared test results with capacitors that were irradiated using a progressively increasing series of voltage conditions (multiple irradiations) with experiments done on fresh capacitors that were not previously irradiated, with no apparent difference. Thus, it is more likely that the ions have to strike a small critical region of the device *when the applied field is high enough to cause breakdown at those sites* in order for breakdown to occur. This is consistent with the features of extrinsic breakdown in the TDDDB studies of Reference 4 that are related to oxide impurities; the fraction of devices that fail after a fixed time interval increases with higher field strength. Thus, the field strength at which the capacitors break under TDDDB depends is not unique, but depends on the capacitor area and time.

Using the mean number of ions required for breakdown, one can determine the effective fractional area for the breakdown process (the number of ions indirectly determines how small the area near a defect can be that is “probed” by the experiment). For experiments with intermediate fluences, the effective area is about $2 \times 10^{-5} \text{ cm}^2$ for the 75 Å capacitors, and 10^{-5} cm^2 for the 45 Å capacitors. This effective dimension for breakdown may simply be due to the average distance between the effective number of defects that are involved, or it may be related to both the defect density and the localized distance from each defect in which a heavy ion will cause breakdown to occur.

When the same experiments were repeated at high fluence, the effective fractional area for breakdown decreased substantially. This would not occur if breakdown was associated with a finite number of defect sites. However, the critical voltage was also lower. One way to interpret this is that the higher fluence increases the probability of hitting even weaker defect locations, which have lower critical fields, but are present in smaller numbers (as indicated by TDDDB data in the literature [8-14].

B. Random Behavior

One important question is whether failures in the capacitors are truly random events, not associated with the edge of the capacitor or its previous radiation history, and are caused by the passage of a single ion rather than the superposition of effects from two or more ions. The flux rate used in our experiments was low enough so that any effects from multiple ions would have to involve residual damage, not transient effects from ions striking the oxide simultaneously.

Although diagnostic measurements of breakdown site locations after breakdown showed that the perimeter was not involved in typical ion-induced breakdown, this does not directly address the statistical question. If events are truly random, then the breakdown should obey Poisson statistics. For a Poisson process, the number of capacitors that survive a specific fluence (N_{surv}) should obey the equation

$$N_{\text{surv}} = N_0 \exp(-\sigma_f \phi A_c) \quad (1)$$

where N_0 is the number of capacitors, σ_f is the fractional area that is affected by breakdown, ϕ is the total fluence, and A_c is the capacitor area.

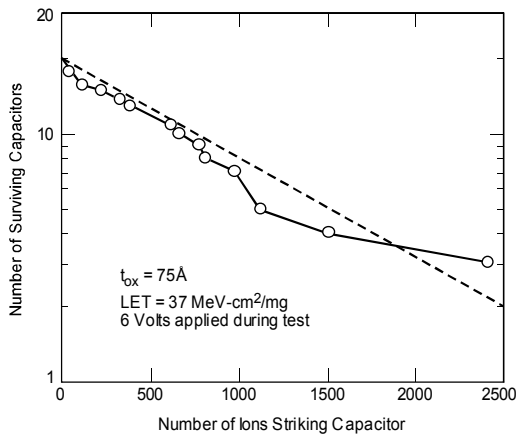
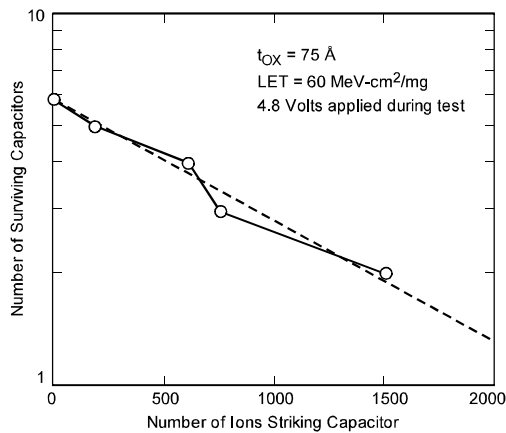
Semilogarithmic plots of the number of surviving capacitors vs. fluence are shown in Figure 7 for 75 Å oxides at two different LETs. The data are a reasonable fit to a straight line, implying that Poisson statistics apply to the breakdown process. Results from tests at higher fluences were similar (with lower voltages and much higher fluence values). These results add further credibility to the assumption that breakdown is the result of a single ion interaction, with no dependence on residual damage from previous ion strikes, even for the high-fluence tests where the vast majority of ions that pass through the oxide do not cause gate rupture.

Another important issue is whether breakdown occurs in random locations, or is heavily influenced by edge effects where the electric field is somewhat higher. Figure 8 shows a representative example of defect site after irradiation with heavy ions, determined with a liquid crystal technique that can detect very small changes in temperature (the aluminum over the top of the poly did not allow light emission techniques to be used). The sample shown in the figure was irradiated with approximately 1000 ions before breakdown occurred (intermediate fluence). A small current was allowed to flow in the capacitor during this diagnostic measurement, which was done several weeks after the heavy ion tests. The position and approximate size of the defect is determined by polarization changes in the crystalline material, which coats the surface for the diagnostic test (the technique only detects thermal changes, and the actual size of the defect is probably somewhat smaller than indicated).

The defect is well removed from the edge, and appears to be associated with a relatively small thermally heated region (about 2-5 μm) based on a CCD detector with an optical microscope.

Figure 7. Semilog plot of the number of surviving capacitors vs. fluence for two different LET values.

Figure 8. Representative oxide damage site observed with liquid crystal diagnostics after gate rupture had occurred

(a) LET = 37 MeV-cm²/mg(b) LET = 60 MeV-cm²/mg

The similarity of results with fresh capacitors to those with previous radiation history, the diameter measurements and the Poisson-like failure statistics all support the conclusion that breakdown is caused by the passage of a single ion through the capacitor structure. The number of ions required and the dependence on fluence suggests that the ion must strike close to small regions within the capacitor that are more sensitive to breakdown; the effective area of the oxide that is sensitive to breakdown depends on applied field.

Capacitor area is also a factor. We attempted to eliminate this variable in our experiments by adjusting the flux so that each capacitor was exposed to the same number of ions during each test run. There was no apparent difference in the critical fields for our capacitors within the limited range of areas that were available. The statistics of the breakdown process limit the ability to determine area dependence unless very large numbers of capacitors are tested (see Figure 7). However, the number of defects is also related to capacitor area. TDDDB studies [8,9] have shown that the extrinsic defect region (see Figure 1) is generally not observed for capacitors with area below about 10^{-6} cm². They attribute this to the physical distribution of defects, which implies that capacitors with small area have a much lower probability of containing defects that significantly lower the oxide breakdown.

Extending this argument to gate rupture, the critical field may also be lower for capacitors with large area. However, the presence of a small number of defects in large area capacitors is less important for gate rupture in space because gate rupture cannot occur unless the ion strikes in close proximity to the defect. The probability of gate rupture depends on the fluence and the effective defect area. Defect sites with lower breakdown are more important for TDDDB because TDDDB stresses the entire oxide area, not just the localized region of an ion strike.

C. Breakdown in Very Thin Oxides

Another important topic is the breakdown signature of the capacitors. None of the breakdown events in the capacitors produced true short circuits. Breakdown produced a resistive path, on the order of 10 to 200 kohms, in the capacitor. Current steps associated with the breakdown were in the range of 80 to 1200 μ A for the 75 Å capacitors, and 10 to 100 μ A for the 45 Å capacitors. In cases of low current breakdown it was sometimes possible to observe more than one breakdown event during a heavy ion test because a large voltage could still be sustained across the device without destroying it. Radiation tests must be capable of detecting currents in the μ A region, as well as distinguishing between hard and soft breakdown.

The soft breakdown characteristics of the 45 Å capacitors are very similar to the breakdown characteristics reported in the reliability literature for TDDDB [10-13]. Those results show that soft breakdown is the dominant mechanism for very thin oxides, and it is likely that heavy ions will produce similar characteristics in very thin oxides. Such breakdown events may be difficult to measure in radiation experiments. Oxides as thin as 15 Å have been proposed, where direct tunneling allows significant current flow in the gate [14].

D. Effects on Scaled Devices

The issue of how the gate rupture problem is related to device scaling is a very complex problem. Very high fields – 6 MV/cm or more – have been proposed for future devices [7,15], and the significance of gate rupture in devices will likely depend on how far the electric field strengths are pushed in future device technologies. Sexton, et al. [3] noted that oxide defects will have to be reduced in order to make useable devices at high fields, which may make scaled devices less susceptible to gate rupture. However, very few oxides have been subjected to gate rupture experiments, and most of the conclusions about scaling are based on experiments with capacitors. As noted earlier, although capacitors provide insight into some aspects of the phenomena, they cannot necessarily be extended directly to circuits because of the difference in geometry and doping levels.

Results from radiation tests of gate rupture on thin oxides are compared for several different device types in Figure 9. These comparisons are made at an LET of 60 MeV-cm²/mg; the intent is to show how results on various devices compare, and how they relate to circuit voltages. Maximum voltages for 3.3 and 5 V logic are also shown.

The capacitor data of Sexton, et al. [3] lie on a straight line. Their tests of a commercial SRAM departed somewhat

from the capacitor results, which could be caused by differences in area (the 256 kB SRAM likely has considerably greater total oxide area than the capacitors) or by the fact that the SRAM is manufactured with a different process. The results for our capacitors show significantly lower critical voltages than for the capacitors tested by Sandia. The difference appears to be consistent with the decreased critical voltage observed for the SRAM in the Sandia work (the dashed line is only intended to show that consistency, not to imply that the processing is the same). The older 4-Mb DRAM results show even lower critical fields; that may be related to the complex processing steps required for DRAM capacitors[17] or to differences in the oxide quality.

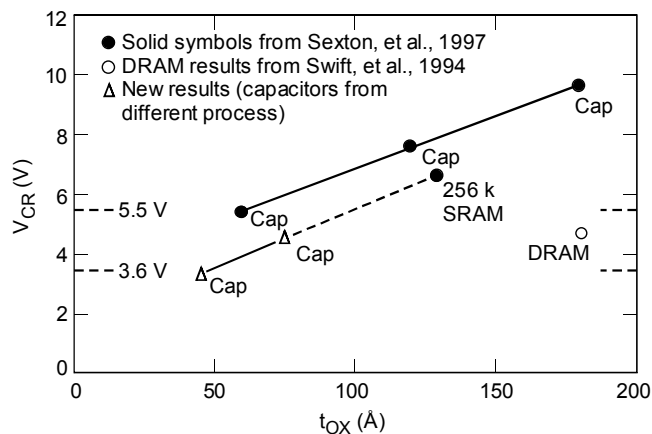


Figure 9. Critical voltages for gate rupture for several different technologies.

The results in Figure 9 show that there are substantial variations in the critical voltage for gate rupture for various devices. Part of the difference may be due to different test conditions and fluence levels. Although oxides produced in some device manufacturing processes clearly have sufficiently high critical fields to be immune to gate rupture, the fields of the more sensitive oxides are in the range of 5-6 MV/cm for ions with high LET which is the approximate range of electric fields that are projected for future MOS devices from scaling studies [7,15,17]. Thus, it is possible that some devices may be affected by gate rupture even when they use thin oxides. This will depend on many factors, including the issue of whether projected scaling trends are really implemented.

More work is needed to understand the mechanisms and the relationship of gate rupture sensitivity to processing and device design. This is particularly important because of the trend towards adapting commercial devices for space, with no control and limited knowledge of device processing and design. Fortunately, the critical fields appear to be high enough for most devices so that only ions with high LET – well beyond the “iron threshold” where there are very few particles in space – can cause gate rupture. However, it may still be important for systems with large numbers of VLSI devices, which is the trend for many modern space systems.

V. CONCLUSIONS

The results in this paper show that gate rupture in scaled devices is a complex problem that is not fully understood. Processing details and oxide defects appear to play a role in gate rupture, and the differences in experimental observations by different groups may be due solely to differences in semiconductor processing. However, experiments done to date have generally shown that many ions must pass through the oxide region before breakdown occurs. When gate rupture occurs, it appears to be associated with a single ion, but not all of the ions are equally effective in producing rupture. This implies that there is an effective region near the defect where the ion strike can cause breakdown at lower fields than in regions where defects are not present.

The critical field is not uniquely defined, but depends on the fluence used during “steps” in the experimental characterization of gate rupture. If the fluence is too low, then the critical field may be overestimated by as much as 15%. This is a potential source of ambiguity and confusion in comparing different test results.

For some processes, the critical field appears to be low enough for gate rupture to occur within the range of anticipated power supply voltages for scaled devices. Even though thin oxides appear to have higher critical fields, the electric field is also projected to increase for scaled devices. The ultimate importance of this effect may depend on how high the internal oxide fields eventually become in practical devices.

Soft breakdown dominated the behavior of the 45 Å capacitors, but not in 75 Å capacitors. Soft breakdown produces small changes in current that result in breakdown, but do not have the abrupt, low resistance characteristic that is usually associated with oxide breakdown. Equilibrium currents that occur after breakdown are relatively small, and difficult to measure during test with heavy ions. However they are large enough to cause circuit failure if they occur internally in small-area devices within VLSI circuits. Although the mechanism for soft breakdown is different than for abrupt breakdown in thick oxides, the critical voltage for soft breakdown was consistent with projections from breakdown in thicker oxides taking oxide thickness and electric field into account.

Gate rupture in thin oxides is an interesting topic, but it has been studied for relatively few devices and processes. More work needs to be done to increase the level of understanding as well as how it may affect highly scaled commercial devices in space.

REFERENCES

- [1] G. M. Swift, D. J. Padgett, and A. H. Johnston, “A New Class of Single Event Hard Errors,” *IEEE Trans. Nucl. Sci.*, **41**, p. 2043, December 1994.
- [2] G. Swift and R. Katz, “An Experimental Survey of Heavy Ion Induced Dielectric Rupture in Actel Field Programmable Gate Arrays (FPGAs),” *RADECS95 Proceedings*, IEEE Pub. 95TH8147, p. 425, 1995.

- [3] F. W. Sexton, D. M. Fleetwood, M. R. Shaneyfelt, P. E. Dodd and G. L. Hash., "Single Event Gate Rupture in Thin Gate Oxides," *IEEE Trans. Nucl. Sci.*, 44, p. 2345, December 1997.
- [4] F. B. McLean and T. R. Oldham, "Charge Funneling in n- and p-Type Substrates," *IEEE Trans. Nucl. Sci.*, 29, p. 2018, December 1982.
- [5] P. E. Dodd, F. W. Sexton and P. S. Winokur, "Three-Dimensional Simulation of Charge Collection and Multiple-Bit Upset in Si Devices," *IEEE Trans. Nucl. Sci.*, 41, p. 2005, December 1994.
- [6] J. L. Brews, K. K. Ng and R. K. Watts, "The Submicron Silicon MOSFET," chapter 1 in *Submicron Integrated Circuits*, R. K. Watts (Ed.), New York: John Wiley, 1989.
- [7] B. J. Davari, "CMOS Technology Scaling, 0.1 μ m and Beyond," 1996 IEDM Technical Digest, p. 555.
- [8] R. Degraeve, J. L. Ogier, R. Bellens, P. J. Roussel, G. Groeseneken, and H. E. Maes, "A New Model for the Field Dependence of Intrinsic and Extrinsic Time Dependent Breakdown," *IEEE Trans. Elect. Dev.*, 45, p. 472, February 1998.
- [9] R. Degraeve, G. Groeseneken, R. Bellens, J-L. Ogier, M. Depas, P. J. Roussel and H. E. Maes, "New Insights in the Relation Between Electron Trap Generation and the Statistical Properties of Oxide Breakdown," *IEEE Trans. Elect. Dev.*, 45, p. 904, April 1998.
- [10] D. J. Demaria, "Defect Properties and Breakdown of Silicon Dioxide Films," *Solid St. Elect.*, 41, No. 7, p. 957, 1997.

- [11] S-H. Lee, B-J. Cho, J-C. Kim and S-H. Choi, "Quasi-Breakdown of Ultrathin Gate Oxide under High Field Stress," 1994 IEDM Proceedings, p. 605.
- [12] M. Depas, T. Nigam and M. Heyns, "Soft Breakdown of Ultra-Thin Gate Oxide Layers," *IEEE Trans. Elect. Dev.*, 43, p. 1496, September 1996.
- [13] B. Weir, P. J. Silverman, D. Monroe, K. S. Krisch, M. A. Alam, G. B. Alers, T. W. Sorsch, G. L. Timp, F. Baumann, C. T. Liu, Y. Ma and D. Hwang, "Ultra-Thin Gate Dielectrics: They Break Down, but Do They Fail?," 1997 IEDM Proceedings, p. 73.
- [14] H. S. Momose, S. Nakamura, T. Ohguro, T. Yoshitomi, E. Morifuji, T. Morimoto, Y. Katsumata and H. Iwai, "Study of the Manufacturing Feasibility of 1.5 nm Direct-Tunneling Gate Oxide MOSFETs," *IEEE Trans. Elect. Dev.*, 45, p. 691, May 1998.
- [15] S. Asai and Y. Wada, "Technology Challenges for Integration Near and Below 0.1 μ m," *Proc. of the IEEE*, 85, p. 505, April 1997.
- [16] G. J. Johnson, K. F. Galloway, R. D. Schrimpf, J. L. Titus, C. F. Wheatley, M. Allenspach and C. Dachs, "A Physical Interpretation for the Single-Event-Gate Rupture Cross Section of N-Channel Power MOSFETs," *IEEE Trans. Nucl. Sci.*, 43, p. 2932, December 1996.
- [17] H. Ishiuchi, T. Yoshida, H. Takato, K. Tomioka, K. Matsuo, H. Momose, S. Sawada, K. Yamazaki and K. Maeguchi, "Embedded DRAM Technologies," 1997 IEDM Technical Digest, p. 33.

